FIG. 1
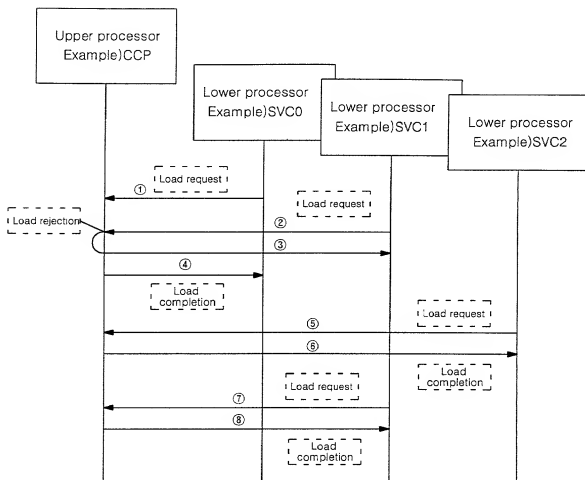
BACKGROUND ART

FIG. 2

BACKGROUND ART

Information contained in a memory of
a upper processor

```
typedef struct{
        int         zip_add_start;
        short       ld_sts;
        char        unzip_sts;
        int         zip_len;
        int         pack_no;
        short       last_len;
        char        ldfname[12];
        short       ld_sts;
        int         start_addr;
        unsigned    chk_sum1;
        unsinged    chk_sum2;
        char        version[32];
        char        data[MAX_IPC]
}T_MutiLoad;
```

Pre-defined IPC format

Destination Address	4bytes
Source Address	4bytes
Type	1byte
Control	1byte
Sig ID	2bytes
Length	2bytes
Data	200bytes

FIG. 3

Address of 4bytes

NA
BA
CA
SA

NA(Node Address) : Processor element ID
BA(BHIU Address) : Processor ID
CA(Cinu Address) : Network group ID 1
SA(Slot Address) : Network group ID 2

FIG. 4

Starting up down-load — S1

Accessing memory — S2 ← once access

Is there an error? — S3
Yes
No

Grouping representative address — S4

Creating message — S5 ← Pre-defined IPC format

S6 — Transferring the message ← 1. Using the grouped representative address
2. Multiplexing mode down-load algorithm

S7 — Processor ← A plurality of processor are down-loaded with program or data at the same time